Addressing future trends in integrated silicon photonics

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Silicon Photonics: Rationale

What’s the big idea about silicon photonics?

- **What:**
  - Integrated photonic circuits on silicon using CMOS foundry facilities

- **Why:**
  - Cost of production
  - Power consumption efficiency
  - System footprint
  - Alternative market not fully addressed by III-V discrete photonics
  - New markets out of data-communication

- **Opportunities:**
  - Knowhow ➔ Among the more explored & mastered areas of science
  - Throughput ➔ Large volume manufacturability
  - Robustness ➔ Resist to a wide variety of perturbations
  - Reliability ➔ Long lifecycle when operated within specifications

- **Constraints:**
  - Process flow ➔ Fabrication flow must be compatible with existing technologies
  - Contamination ➔ Strict regulations about: material contamination, health hazards, safety hazards
    - Some materials not allowed (III-V, Fe,...)
    - Some materials in restricted zones (FEOL / BEOL: Cu, Au,...)
Optical Communication Trend

Fiber optics data communication evolution

Optical link network keeps on getting denser.

So far, the market still addresses the professional market.

Projections tend towards intra processor core optical communication.

Ultimately, we may converge towards a model where:

Logic ➔ Electrical charges
Communication ➔ Photons
Storage ➔ ions

Communication at which ever scale is technically potentially feasible. It won’t happen without silicon photonics.
New opportunities in silicon photonics

Silicon photonics cannot rely on data communication professional market only.

For the industry to develop:
- More applications
- Huge volumes
- More actors
- Bigger competition
- Lower prices
- More innovation

However, the applications, even though dissimilar, should make use of almost the same technology.
Mixing up future silicon photonics systems will potentially lead to even better innovation:

Typically, a trend in automation is to have robots substituting to humans. Digital logic + photonics communication + photonics sensor ≈ neuronal network + nervous network.

→ Rapid detection, rapid dispatch, rapid analysis of information.

→ Applications: Autonomous cars, airplanes, trains,…

More than Moore: Diversification
- Analog/RF
- MEMS
- Imaging
- Power
- Silicon Photonics

More than Datacom: Diversification
- Datacom
- Internet Of Things
- Connecting Objects
- Sensors
- Detectors
- Information Collection
- Information Transport
- Ultra Fast Reach of Information
- 10Gbps
- 40Gbps
- 100Gbps
- 200Gbps
- 400Gbps
- 1Tbps
- …

Combining SoC and SiP: Higher Value Systems
- Digital content System-on-Chip (SoC)
- Non-digital content System-in-Package (SiP)
- Information Processing
- Information Storage
- Baseline CMOS: CPU, Memory, Logic
- More Moore: Miniaturization
- 14nm
- 22nm
- 32nm
- 45nm
- 65nm
- 90nm
- 130nm

Dr. Charles Baudot  STMicroelectronics  Silicon Photonics R&D
R&D Programs:

PLAT4M

PARTNERS

CEA-LETI
IMEC
STMICROELECTRONICS STD CROLLES
STMICROELECTRONICS MPD AGRATE
TNO
MENTOR GRAPHICS
PHOENIX
III-V LABS
UNIVERSITY COLLEGE CORK, Tyndall
POLYTEC
THALES
UNIVERSITE PARIS-SUD
AIFOTEC FIBEROPTICS
NXP SEMICONDUCTORS
SI2

Funding:
Project Description

- **Project full title:** "Photonic Libraries And Technology for Manufacturing"

- **Project Description:** PLAT4M's objective is to bring existing silicon photonics research platform to a maturity level which enables seamless transition to industry, suitable for different applications fields and manufacturing volume levels.

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<th>CEA-LETI</th>
<th>IMEC</th>
<th>STMicroelectronics</th>
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<tr>
<td>SYLPHIDE 200mm MPW</td>
<td>ISIPP25G 200mm MPW</td>
<td>DAPHNE 300mm R&amp;D Platform</td>
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Tyndall National Institute

Assembly & Packaging Solution
Technology Setup

Building up a new technology

Derivative technologies (diversification) are usually launched using existing processes. DAPHNE (Datacom Adv. Photonics Nanoscale Env.) is a technology meant for R&D.

Both the process and device library evolves.

The current and predicted production volumes are the main arguments that usually decide about the amount to be invested in innovation.
Process building blocks compatible with a CMOS foundry

**Process:**

The fabrication flow is divided into building blocks so that process development work is done in parallel. The integration activity ensures that the blocks are compatible with each other.

**Device:**

While passive devices are all fabricated in a single block, active devices involve the whole flow.

Different technologies coexist within the same foundry. Tools are qualified to be shared among those technologies.
Silicon Patterning

Photonics Integrated circuits

Target:
Etch silicon so as to define photonic devices & circuits

Challenge:
- Auto-alignment between all devices at chip level
- Partial etching of silicon with good uniformity
- Non-Manhattan architectures
- Huge disparity in targeted lateral dimensions & morphologies

Multi-level patterning of silicon is a more than CMOS process building block developed for silicon photonics

- Step 1:
  - High resolution patterning step to define the global photonic path in a single step (auto-alignment)
- Step 2:
  - Low resolution patterning step to locally etch further silicon
- Step 3:
  - Low resolution patterning step to locally protect silicon from etching

350nm strip IL: 3.5 dB/cm
320nm deep-rib + 50nm slab IL: 3.7 dB/cm
400nm mid-rib + 160nm slab IL: 1.4 dB/cm

The inset shows the waveguide after the whole process.
Silicon Patterning

Multi-level silicon patterning development to address device requisites
Germanium Integration

High Speed Photodetector

New material integration is a challenge in a CMOS foundry. Besides contamination issues, process feasibility must be established.

Mono-crystalline germanium includes:

- Selective epitaxial growth of Ge using a Si seed masked by SiO₂.
- Si/Ge lattice mismatch.
- Thermal budget of Ge.
- Chemical compatibility (Ge oxidizes easily. GeOₓ is soluble in water).
- Same implantation strategy as silicon.
- Same BEOL of Si devices.

(10 X 15) µm pure mono-crystal Ge obtained by selective epitaxial growth using a patterned silicon seed masked by silicon dioxide.

Interface between germanium and silicon layers showing a good Ge crystal quality.

Right part of Ge pin photodiode with 3 interconnect metal layers.
Photonic Integrated Circuit

Schematics of a typical PIC

Passive Devices
- Waveguides, Grating couplers, directional couplers, AWG, MMI,...

Active Devices
- Standard rib high speed PN depletion junction
- Standard rib low loss PIN injection junction

Far-BEOL
- Cu Posts

BEOL
- 3 interco Cu lines
- 1 RF Cu line
- 1 RF Al line

Active Device
- High speed Ge side coupled integrated photo-detector

Active Devices
- Deep rib high speed PN depletion junction
- Deep rib low loss PIN injection junction
Copper posts and copper pillars are grown on the metal pads.

Bonding is done by die-to-wafer flip chip of the EIC on the PIC.

Copper pillars allow direct connection between the middle of the two dies (No routing to die edge).
Test Vehicle: 100GBase-LR4 Demo

Integrated Multiplexed Transmitter

100GBase-LR4 transceiver system.

WDM device designed and simulated: Array Waveguide Grating.

Stand-alone device shows a loss of 1.2 dB / channel

Device integrated in system. Fabrication On-going.
R&D Programs:

IRT Project 2012 - 2018

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Funding:
• **Project full title:** "Institut pour la Recherche Technologique"

• **Project Description:** Bring together in a single organization all the tools and know-how to develop silicon photonics solutions that can address a wide variety of applications.
It is not clear yet whether an integrated laser at wafer level will correspond to all needs in optical data communication.

System providers militate in favor of different approaches.

Main parameters for DATACOM:
- Cost
- Footprint
- Power consumption
- Reliability
- Robustness

In alternative markets, the constraints are different. Moreover, the need of an integrated source is very likely.

Whatever the application, it is very probable that an integrated source will be coveted in future silicon photonics.
Typically 3µm thick III-V bonded to SOI waveguide.

Close proximity (~100nm) needed between III-V and Si 500nm waveguide.

Surface preparation prior to bonding based on CMP, preventing topography on Si photonics wafer.

Topographical problem: similar heights (~3µm) of laser and 4 level metal stack.

Planar surfaces needed (CMP) for III-V/Si bonding and 4 level Cu back-end.

The idea: use flat back-side of Si waveguide for laser integration.

Si device interconnects on one side, III-V/Si laser on other side.
Source Integration

Integrated III-V Laser

Distributed Bragg Reflector hybrid III-V/Si laser cavity emitting at 1310nm

Active region: optical mode confined in the III-V waveguide

Mirror: DBRs in the Si on both side of the III-V

Or any other more complex silicon photonic sub-system: modulator, Mux,…
Source Integration

Integrated III-V Laser

Light transferred by adaptation of effective index using the super-mode theory:

Variation of the SOI waveguide rib’s width (W_{rib}) along the propagation direction.

Over 97% of the light is transferred to the single-mode waveguide

Source Integration

Integrated III-V Laser

SOI wafer level III-V bonding strategy:

Preliminary tests done by wafer-to-wafer bonding

Ongoing developments to bond locally patches of III-V material
R&D Programs:

H2020 Project 2015 - 2018

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<td>UNIVERSITY OF ST ANDREWS</td>
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Funding:
- **Project full title:** "CmOs Solutions for Mid-board Integrated transceivers with breakthrough Connectivity at ultra-low Cost"

- **Project Description:** COSMICC consortium will achieve mid-board optical transceivers in the [2Tbit/s, 2pJ/bit, 0.2$/Gbit/s cost]-range.

![Diagram showing 24 channels, 24 Fibers I/O, 12 X 4 X 50 = 2400Gbps]
Project Description

COSMICC-H2020 Project

- Project Organization:
Capacitive Modulators

Capacitive structures substituting junctions

**Vertical Integration**
1.6pF/mm capacitance oxide ([3;10]nm oxide thickness range)

1.2Vpp voltage swing ([0.6-1.8]V) with a DC bias to put swing around flat-band voltage and use accumulation charges

⇒ 1.52pJ/bit at 56Gb/s

**Horizontal Integration**
1.1pF/mm capacitance oxide ([5;15]nm oxide thickness range)

0.9Vpp voltage swing ([0.9-1.8]V) with a DC bias to put swing around flat-band voltage and use accumulation charges

⇒ 0.37 pJ/bit at 56Gb/s

Push-pull MZI with 30° phase shift on both branches:
⇒ Active Length <1mm
Summary & Conclusions

• New feature in CMOS: wafer size did not evolve for more than one and a half decade.
  • Traditionally, old tools were used for diversification (Ex: MEMS). It is not the case for silicon photonics.
  • Silicon photonics shares the same 300mm fab tools as other high-end technologies. Strict regulations about tool contamination or deviation.
  • Process evolution, new material introduction and device integration are all technically possible but not under any conditions.
  • Silicon photonics is a promising market and strategic efforts must be done to cover a wide variety of applications.