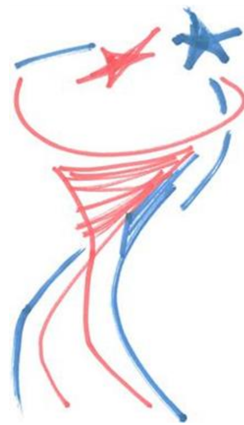
ICT - Information and Communication Technologies



PhoxTroT

Photonics for High-Performance, Low-Cost & Low-Energy Data Centers, High Performance Computing Systems: Terabit/s Optical Interconnect Technologies for On-Board, Board-to-Board, Rack-to-Rack Data Links

Collaborative Project
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2.5 and 3D integration path for PhoxTroT optochip D8.2

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Abstract:
The purpose of this deliverable is the demonstration of the capability of all partners to build 2.5D and 3D optical chips and the capability for chip to board and board to board communication. Optical chip is the name for a platform or interposer that serves as base for the mounting of components with optical and electrical functionality. These components comprise further chips with special functionalities like photo diodes for receiving optical signals, VCSELs (vertical cavity surface emitting laser) for the emission of light signals and TIAs and drivers for the processing of electrical signals and the control of the optical devices. 2.5D means only a semi 3D solution with all the components mounted on the same side without the need of signal transfer from one side of the interposer to the other; this will serve as fall-back solution. The main target is the so-called 3D solution, where also the backside of the interposer is used for the assembly of components while through silicon vias (TSVs) serve as a transmitter for electrical and optical signals from one side to the other.

Keywords: PCB, TSV, wave guide, optical coupling loss

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Table of Contents

1 Executive Summary 5
1.1 Document structure 6
1.2 Audience 6
2 Chip to board (C2B) process flow design 6
2.1 Summary 6
2.2 AMO KIT version (Silicon-organic hybrid (SOH) switches) 6
2.2.1 Process flow (200mm wafers) 6
2.2.2 Critical Steps 8
2.3 UP Valencia version (Carrier depletion pn Si-photonic e/o switches) 10
2.3.1 Process flow 10
2.3.2 Critical Steps 12
2.4 ePIX option 12
2.4.1 Process flow 12
2.4.2 Critical Steps 13
2.5 PN carrier depletion switch with cooperation of UPVLC-AMO-AMS 13
2.5.1 Process flow 13
2.5.2 Critical Steps 15
2.6 Risk Assessment 15

1 Executive Summary

The objective of deliverable D8.2 was the finalization of the process flow. Two competing options for optical switches were defined at the beginning of the project in task 6.1, the more suitable kind of switch was then planned to be realized. On the one hand a silicon-organic hybrid switch (SOH) is delivered from a cooperation of AMO and KIT and on the other hand UPVLC can supply carrier depletion pn Si-photonic e/o switches. Unfortunately both options have severe disadvantages for the integration. The processing of wave guides (and switches) is rather at the beginning of the process flow, but during TSV processing and the assembly of the optical and electrical components, temperature budgets up to 400°C are applied for some processing steps. These are temperatures that the polymer in the SOH switch cannot stand. Therefore a significantly more complicated process flow had to be set up, where the polymer filling of the switches and the poling is placed after the assembly. The second approach for optical switches, the carrier depletion pn switches, is more suitable for the integration into a process chain with TSVs and assembly, but unfortunately these kinds of optical switches can only be supplied by UPVLC on 150mm wafers, while the interposer processing at AMS is only possible with 200mm wafers. A work-around with bonding of 150mm wafers to 200mm wafers is only possible with the support by external resources (no project partners) and high risk in the AMS fabrication.
A third option which could solve the problem with the wafer size incompatibility between UPVLC and AMS was the realization of the carrier depletion switches designed by UPVLC on 200mm wafer in the ePIX foundry service.
Due to the problems faces by these three options a tiger team led by AMS with IZM, AMO, KIT, UPVLC, CERTH, DAS as team members was defined. The task was the evaluation of the different options, the creation of alternative processing paths and the final decision about the technology to be used. The outcome was surprising but nevertheless a conclusive solution. In a forth option the following processing scheme was agreed. The carrier depletion switch technology was chosen because of the compatibility of the pn junctions produced with doped Si material with high temperature processing which is needed for the interposer processing. The only possibility of the usage of organic material as it is indispensable for the SOH approach, was the deposition and poling of the organic material after the interposer processing. This imposes a big amount of development work and a high risk if the final process is feasible at all. The wafer size incompatibility between UPVLC and AMS will be overcome by the usage of AMO as foundry for the UPVLC design. AMO is only partially capable of 200mm processing. The missing processing step comprising especially doping annealing and contacting of the pn junction areas will be contributed by AMS.

1.1 *Document structure*

1.2 *Audience*

This document is internal to PhoxTroT project consortium.

2 Chip to board (C2B) process flow design

2.1 *Summary*

The process flow, risk assessment and evaluation for the four processing options (SOH approach by AMO & KIT, the carrier depletion approach by UPVLC, carrier depletion processed by ePIX, cooperation UPVLC-AMO-AMS) will be presented.
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2.2 *AMO KIT version (Silicon-organic hybrid (SOH) switches)*

2.2.1 Process flow (200mm wafers)

The starting material is a 200mm SOI wafer with 220nm Si on 2µm Si oxide. The structuring of the wave guide layer in order to create all necessary optical functionality as switches, modulators, grating couplers etc. will be done by AMO. All structures are already tested on 150mm wafer or on die basis, as AMO has a complete flow for 150mm wafers, including also etching, doping and annealing. While the etching of 200mm wafers is capable for AMO after changing the chuck of the etcher, the doping by implanters and the annealing can only be done by AMS as AMO has this kind of equipment only available for 150mm wafer. Implanters and annealing equipment are front-end equipment (all processing steps before the metallization) and are therefore especially critical in respect to cross-contamination.

The back-end metallization with intermetal dielectricum will be delivered by AMS. The contact module has to be adjusted to the needs of the wave guide structures, but as it is a contact to Si, it can be done with the same process module as the standard contacts. After finishing the back-end processing, the passivation and the bond oxide deposition, the first temporary handling wafer is bonded. This handling wafer supports the interposer wafer sufficiently in order to grind and polish the substrate to the final thickness of less than or equal to 200µm. The TSVs will be etched and provide an electrical contact to the metal 1 layer on the wave guide side of the interposer. An additional mask step will be needed in order to define the openings for the deposition of the organic cladding material of the wave guide switches (named "wave guide window" in the following). The most promising kind of way would be to do the deep reactive ion etch together with the TSV etching and then do the oxide etch masked in such a way that the openings of the wave guide window are not oxide etched. The oxide etch would have to be done later, e.g. after the finalization of the passivation, in a two step process. First a fast RIE step and second a wet clean that would protect the surface of the wave guide, as any roughness on the wave guide surface would deteriorate the light transmission.

Finally the TSV metallization is processed and a passivation layer is finalizing the TSV processing. The second temporary handling wafer is then bonded to the TSV side of the

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interposer wafer, helps to stabilize the interposer stack and covers the TSVs and wave guide windows. Thus the first temporary handling wafer can be removed and the wave guide side of the optical chip is released and freely accessible again. By a masked etching process the bonding pads on the wave guide side are released.
Now two options are available. Firstly the UBM (under bump metallization) on the wave guide side is processed by IZM with the temporary bonding wafer from AMS. Then a thermal slide off would have to be done by IZM. This is difficult because of the high UBM topography up to 50 µm. A special rubber chuck is needed for this process. Evaluations on test wafers have been started.
Secondly the wafer is de-bonded by AMS without high topography and sent to IZM as thin wafer. IZM is doing a temporary bonding again on a glass wafer. In this case the de-bonding can be done by laser exposure. As no horizontal forces are needed for the de-bonding it is less critical in respect to topology.
After the UBM process on the wave guide side and the de-bonding, the dies are singulated and stud bumps are placed on the Al pads on the TSV side. Thermo compression bonding will be done on the wave guide side with VCSELs and PDs, while the drivers and TIAs are bonded on the TSV side. Then the interposer together with all components is bonded to the PCB.
As the polymer is a very temperature critical component, it has to be applied at the end of the process flow. TSV- but also the thermo compression bonding-process would destroy this organic material. Therefore the deposition procedure was put in this flow at the end. Of course this implies a very costly and time consumable process as every single die has to be processed separately.

Table1: Process Flow according to the Silicon Organic Hybride Switch Technology (KIT&AMO)

Partner	Level	Process Step	Description	Notes / Risks	Critical for / process indicators
AMO	8" wafer	Start Material	SOI wafer	220nm Si on 2µ BOX	
AMO	8" wafer	Definition Marker layer	i-line Stepper + RIE etching	Possible with Ebeam	
AMO	8" wafer	Definition low doping area	i-line Stepper	Possible with Ebeam	
AMS	8" wafer	Doping + Annealing		Not Possible @ AMO	
AMO	8" wafer	Rib-WG Definition	Ebeam Litho + RIE etching		
AMO	8" wafer	Strip-WG Definition	Ebeam Litho + RIE etching		
AMO	8" wafer	Grating Coupler Definition	Ebeam Litho + RIE etching		
AMO	8" wafer	Definition high doping area	i-line Stepper	Possible with Ebeam	
AMS	8" wafer	Doping and Annealing		Not Possible @ AMO	
AMS	8" wafer	inter level dielectric	oxide deposition + CMP		
AMS	8" wafer	contacting WG	W-Plug technology		Align to AMO marks
AMS	8" wafer	Metallisation	3 metal layers: metal structuring, oxide depo, CMP, W-Plug technology for inter-metal-contact	statement KIT: WG degradation possible, if wafer (structures) see extensive post processing	max. Temp: 420°C. Wafer exposed to vacuum, several process gases, solvent cleans
AMS	8" wafer	passivation, bond oxide	oxide depo, CMP, nitride depo, oxide depo + CMP for best planarisation		
AMS	8" wafer	1st temporary handling wafer bonding	bonded on WG-side		

AMS	8" wafer	thinning of SOI substrate	currently 200µm, target to go to 100µm	100µm deep TSVs to be investigated	interposer thickness, critical for IZM processes
AMS	8" wafer	TSV processing	deep silicon etch, isolation, contact to landing pad, metallisation, passivation	defines also TSV side metal pads, metal re-distribution	max. Temp: 420°C. Wafer exposed to vacuum, several process gases, solvent cleans
AMS	8" wafer	WG opening processing	opening through interposer substrate, clear gaps between WG (SOH switch) from oxide	process development, shortloop runs necessary, risk of WG detoriation	opening must stay clean through IZM process
AMS	8" wafer	2nd temporary handling wafer bonding	bonded on TSV-side		
AMS	8" wafer	removal of 1st temporary handling wafer	exposes WG-side again		
AMS	8" wafer	WG side Padmask	opening of Al-Pads on WG-side		
AMS	8" wafer	de-bonding of 2nd temporary handling wafer	Option: IZM re-uses temporary bonded wafer stack Otherwise: AMS delivers wafer on foil to IZM	pre evaluations planned if AMS de-bonded: WG slots have to be/stay clean	shipment of thin interposer wafer AMS-IZM
IZM	8" wafer	bonding of temporary handling wafer	temporary handling wafer on TSV side necessary. Refer to option of re-use of AMS handling wafer	pre evaluations planned	
IZM	8" wafer	UBM	UBM , Cu / Ni /Au on WG side	TSV side protected	
IZM	8" wafer	de-bonding of temporary handling wafer		high topology on WG side due to 50µm UBM thickness	
IZM	8" wafer	singulation	dicing of interposer wafer	TSV side protected by dicing tape	
IZM	die	stud bumping	on WG side	Specific tooling for double sided bumping required	
IZM	die	bonding of VCSEL, PD	thermo compression bonding of components on WG-side	Thermal and mechanical stress must not be harmful to VCSEL/PD	VCSEL and PD must withstand forces and temperature of 260°C
IZM	die	bonding of TIA, Driver	thermo compression bonding of components on TSV-side		
IZM	die	Mounting of interposer on PCB	thermo compression bonding of interposer on PCB		Max. Temp: 260°C for TC bonding
KIT	PCB	polymer filling	introduce polymer into interposer opening and WG	200 (100)µm deep, 80µm wide, 500-1000µm long trenches in place to get access to WG slots (220nm deep, 100nm wide)	max. allowed temperatur after polymer: 80° at ambient
KIT	PCB	poling	WG electrically connected, Polymer poling @ elevated temperature	180°C @ defined ambient, 50V needed	

2.2.2 Critical Steps

- Cleanliness and functionality of wave guide structure in WG window
  Risk of wave guide surface damage during opening
  Risk of bonding voids because of large opening
  Risk of wave guide surface damage by temporary bonding glue and removal of glue at de-bonding
  Risk of wave guide surface damage by tape sticking and removal process

Risk of damage or contamination of the wave guide window during stud bump process, thermo compression bonding

- Deposition of organic material and poling has to be processed on single chips, which are already bonded to PCB
  Risk of inhomogeneous layer deposition
  Not mass production capable

2.3 *UP Valencia version (Carrier depletion pn Si-photonic e/o switches)*

2.3.1 Process flow

Again the starting material is a SOI wafer with 220nm Si on 2µm Si oxide. But in this case the wafer has a diameter of 150mm. The wave guide structure, grating couplers and pn depletion switches will be produced by UPVLC. As the wafers have a diameter of 150mm, no processing can be done at AMS. Thus the whole back-end process including the contacts, several metal layers with vias, passivation and bond oxide deposition together with planarization has to be processed by UPVLC. Then the 150mm wafer is bonded to a 200mm handling wafer, which has to be done by an external supplier. Neither UPVLC nor AMS is capable of this bonding process. The 150mm wafer will then be grinded at AMS to a thickness of 200µm or less. The TSV processing will be done by AMS in the same way as described in 3.2.1 though the step from the 150mm wafer to the 200mm wafer could cause problems. Resist layers are typically very thin at such high steps. In the succeeding etching steps then uncontrolled etching takes place and these grooves and holes which occur by unwanted etching, are traps and sources for contamination and particles. After finishing the TSV processing the second temporary handling wafer has to be bonded to the thinned 150mm wafer. The resulting stack of two 200mm wafers with a 150mm wafer in between has a gap with a width of 25mm and a height that is equal to the thickness of the 150mm wafer. Then the first temporary handling wafer is removed by grinding and Si wet etch. As the Si wet etch would etch the second handling wafer in the ring-shaped gap area, the handling wafer needs a Si oxide protection layer which is not a show stopper, but imposes further development effort.
After the removal of the first temporary handling wafer, the wave guide side of the interposer is released. A masked passivation etch opens the pads for the bonding of further components. Also for this mask step the step height from the interposer wafer to the handling wafer will cause problems. The removal of the second temporary handling wafer needs some development effort, as during the slide off process on one side a 150mm wafer and on the other side a 200mm wafer has to be fixed.
Finally the thin interposer wafer is sent to IZM. Here the next steps like temporary handling wafer bonding, UBM processing on the wave guide side, de-bonding and singulation of the dies can be done regularly on a 150mm wafer. Stud bumps are placed on the pads of the TSV side, the components like VCSELS, PDs, drivers and TIAs are mounted and last but not the least the interposer with the components is mounted to the PCB. No further processing of the wave guide layer is needed.

Table 2: Process Flow according to the carrier depletion switch technology (UPVLC) on 150mm Wafers

Partner	Level	Process Step	Description	Notes / Risks	Critical for
UPVLC	6" wafer	Start Material	SOI wafer	220nm Si on 2µ BOX	8" AMS interposer process
UPVLC	6" wafer	WG Definition			
UPVLC	6" wafer	Grating Coupler Definition			
UPVLC	6" wafer	contacting WG			
UPVLC	6" wafer	Metallisation	2-3 metal layers	metal 1 must be compatible to AMS TSV landing pad pre-requisites	TSV connection to metal1

UPVLC	6" wafer			passivation, bond oxide	AMS 1st temporary handling wafer bonding
AMS	6"/8" wafer		bonded on WG-side	1st temporary handling wafer bonding	TSV interposer process
AMS	8" wafer	thinning of SOI substrate	currently 200µm, target to go to 100µm	thinning of 6" wafer on top of 8" wafer	
AMS	8" wafer	TSV processing	deep silicon etch, isolation, contact to landing pad, metallisation, passivation	Resist coating processes must be changed partially due to existing topography (100-200mm) around 6" edge . Shortloop wafer must be handled to whole flow to detect tool problems (=show stoppers)	max. Temp: 420°C. Wafer exposed to vacuum, several process gases, solvent cleans
AMS	8" wafer	2nd temporary handling wafer bonding	bonded on TSV-side	8" wafer to be bonded on TSV side of 6"/8" stack combination	removal of 1st handling wafer
AMS	8" wafer	removal of 1st temporary handling wafer	exposes WG-side again	process to be evaluated for removing a 8" substrate from 6"/8" stack combination	
AMS	8" wafer	WG side Padmask	opening of Al-Pads on WG-side	New resist coating process needed.	
AMS	6"/8" wafer	de-bonding of 2nd temporary handling wafer	release 6" interposer wafer from 8" substrate	to be done at external partner from AMS	shipment of 6" thin interposer wafer AMS-IZM
IZM	6" wafer	bonding of temporary handling wafer	temporary handling wafer on TSV side necessary		
IZM	6" wafer	UBM	UBM , Cu / Ni /Au on WG side	TSV side protected	
IZM	6" wafer	de-bonding of temporary handling wafer		high topology on WG side due to 50µm UBM thickness	
IZM	6" wafer	singulation	dicing of interposer wafer	TSV side protected by dicing tape	
IZM	die	stud bumping	on WG side	Specific tooling for double sided bumping required	
IZM	die	bonding of VCSEL, PD	thermo compression bonding of components on WG-side	Thermal and mechanical stress must not be harmful to VCSEL/PD	VCSEL and PD must withstand forces and temperature of 260°C
IZM	die	bonding of TIA, Driver	thermo compression bonding of components on TSV-side		
IZM	die	Mounting of interposer on PCB	thermo compression bonding of interposer on PCB		Max. Temp: 260°C for TC bonding

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2.3.2 Critical Steps

- Back-end processing at UPVLC
  No established back-end metallization process at UPVLC
  Adjustment of the metallization to the needs of TSV landing pads
  Adjustment of the backend stack for the needs of bonding of the first

temporary handling wafer

- Thinning of 150mm wafer which are bonded to a 200mm handling wafer, risk of handling wafer damage
- Stack of 150mm wafer and 200mm wafer has a high step, risk of etch damages
- Temp bonding of 150mm/200mm wafer stack to 200mm wafer results in a 25mm wide region with gap
- Removal of 200mm handling wafer with 25mm gap between the handling wafers
- De-bonding of 150mm wafer from 200mm handling wafer by external supplier
- De-bonding of 150 mm wafer with 50 µm bump topography

2.4 *ePIX option*

2.4.1 Process flow

The idea of using the ePIX option is that we could take advantage of the carrier depletion switch (no organic material, excellent compatibility to the further TSV and bumping process) and would be able to get wafers with processed wave guides with a diameter of 200mm. No wave guide windows that impose huge problems to the succeeding processing steps (compare 3.2.1) and no extra developments in order to make it possible to process a 150mm/200mm wafer stack (compare 3.3.1) are necessary.
The main problem with this option arises from the fact, that usually multi-project services like ePIX are meant to be used for the processing of single dies. The cost for 20 blocks of a size of 10mm x 10mm is 140kEuro (http://www.europractice-ic.com/SiPhotonics_pricing.php). Therefore the processing of several whole wafers is out ot reach for the PhoxTroT project.

Table 3: Process Flow according to the carrier depletion technology (UPVLC) processed on 200mm wafers at ePIX

Partner	Level	Process Step	Description	Notes / Risks	Critical for
ePIX IMEC	8" wafer	Start Material	SOI wafer	220nm Si on 2µ BOX	8" AMS interposer process
ePIX IMEC	8" wafer	WG Definition			
ePIX IMEC	8" wafer	Grating Coupler Definition			
ePIX IMEC	8" wafer	contacting WG	Option: already done by AMS	clear interface to be defined. Cross contamination risks solved. Enough wafer material must be available. Wafer layout available (alignment marks for TSV processing!)	AMS process compatibility
AMS	8" wafer	Metallisation	2-3 metal layers	to be done at AMS, because IMEC uses Copper metallisation	
AMS	8" wafer	passivation, bond oxide	oxide depo, CMP, nitride depo, oxide depo + CMP for best planarisation		
AMS	8" wafer	1st temporary handling wafer bonding	bonded on WG-side		

AMS	8" wafer	thinning of SOI substrate	currently 200µm, target to go to 100µm	100µm deep TSVs to be investigated	
AMS	8" wafer	TSV processing	deep silicon etch, isolation, contact to landing pad, metallisation, passivation	defines also TSV side metal pads, metal re-distribution	max. Temp: 420°C. Wafer exposed to vacuum, several process gases, solvent cleans
AMS	8" wafer	2nd temporary handling wafer bonding	bonded on TSV-side		
AMS	8" wafer	removal of 1st temporary handling wafer	exposes WG-side again		
AMS	8" wafer	WG side Padmask	opening of Al-Pads on WG-side		
AMS	8" wafer	de-bonding of 2nd temporary handling wafer	Option: IZM re-uses temporary bonded wafer stack Otherwise: AMS delivers wafer on foil to IZM	pre evaluations planned if AMS de-bonded: WG slots have to be/stay clean	shipment of thin interposer wafer AMS-IZM
IZM	8" wafer	bonding of temporary handling wafer	temporary handling wafer on TSV side necessary. Refer to option of re-use of AMS handling wafer	pre evaluations planned	
IZM	8" wafer	UBM	UBM , Cu / Ni /Au on WG side	TSV side protected	
IZM	8" wafer	de-bonding of temporary handling wafer		high topology on WG side due to 50µm UBM thickness	
IZM	8" wafer	singulation	dicing of interposer wafer	TSV side protected by dicing tape	
IZM	die	stud bumping	on WG side	specific tooling required for double sided bumping	
IZM	die	bonding of VCSEL, PD	thermo compression bonding of components on WG-side	Thermal and mechanical stress must not be harmful to VCSEL/PD	VCSEL and PD arrays must withstand forces and temperature at 260°C
IZM	die	bonding of TIA, Driver	thermo compression bonding of components on TSV-side		
IZM	die	Mounting of interposer on PCB	thermo compression bonding of interposer on PCB		Max. Temp: 260°C for TC bonding

2.4.2 Critical Steps

- Contacts at AMS to be processed to Ni Silicide: cross contamination risk
- Cost issue

2.5 *PN carrier depletion switch with cooperation of UPVLC-AMO-AMS*

2.5.1 Process flow

This process flow which includes the advantage of the compatibility of the wave guide process with TSV processing and bumping, which is realizable on 200mm wafer throughout the whole process and which is process able by partners of the PhoxTroT consortium was not visible at the beginning of the project, though in the retrospective it seems to be self-evident. A road blocker was the definition of the two competing flow options in Task 6.1. These are the flows as described in this deliverable in 3.2.1 and 3.3.1 and also in the executive summary. This constellation excluded a cooperation of UPVLC and AMO. Furthermore AMO has only limited resources to do the etching of the wave guides structures on 200mm wafers and has no capabilities to do implanting and annealing steps on 200mm wafers. The support of AMS for the processing of the wave

guide structures by implantation and annealing steps is indispensable for the enabling of the process flow option 3.5.1.
Based on the designs from UPVLC for carrier depletion switches the wave guide layer is processed at AMO and AMS. Starting material is a SOI wafer with 220nm Si on 2µm Si oxide. After the processing of the alignment marks, the low doping area has to be defined by a masking process on the i-line stepper. The implantation and activation is done at AMS. Then the wafers are sent back to AMO, where the wave guide structures like grating couplers and switches are defined and etched. Further doping and annealing will take place at AMS. The contacting, the processing of the metal layers, the passivation, planarization, TSV processing etcetera will be done as described in 3.2.1 and 3.3.1, but without neither the needs of wave guide openings as in the SOH option nor the incompatibilities of bonding 200mm wafers to 150mm wafers as in the carrier depletion option of UPVLC without AMO.
The bonding processes at IZM are then done on 200mm wafers.

Table 4: Process Flow according to the carrier depletion technology (UPVLC) processed on 200mm wafers at AMO and AMS

Partner	Level	Process Step	Description	Notes / Risks	Critical for / process indicators
AMO	8" wafer	Start Material	SOI wafer	220nm Si on 2µ BOX	
AMO	8" wafer	Definition Marker layer	i-line Stepper + RIE etching	Possible with Ebeam	
AMO	8" wafer	Definition low doping area	i-line Stepper	Possible with Ebeam	
AMS	8" wafer	Doping + Annealing		Not Possible @ AMO	
AMO	8" wafer	Rib-WG Definition	Ebeam Litho + RIE etching		
AMO	8" wafer	Strip-WG Definition	Ebeam Litho + RIE etching		
AMO	8" wafer	Grating Coupler Definition	Ebeam Litho + RIE etching		
AMO	8" wafer	Definition high doping area	i-line Stepper	Possible with Ebeam	
AMS	8" wafer	Doping and Annealing		Not Possible @ AMO	
AMS	8" wafer	inter level dielectric	oxide deposition + CMP		
AMS	8" wafer	contacting WG	W-Plug technology		Align to AMO marks
AMS	8" wafer	Metallisation	3 metal layers: metal structuring, oxide depo, CMP, W-Plug technology for inter-metal-contact		max. Temp: 420°C. Wafer exposed to vacuum, several process gases, solvent cleans
AMS	8" wafer	passivation, bond oxide	oxide depo, CMP, nitride depo, oxide depo + CMP for best planarisation		
AMS	8" wafer	1st temporary handling wafer bonding	bonded on WG-side		
AMS	8" wafer	thinning of SOI substrate	currently 200µm, target to go to 100µm	100µm deep TSVs to be investigated	interposer thickness, critical for IZM processes
AMS	8" wafer	TSV processing	deep silicon etch, isolation, contact to landing pad, metallisation, passivation	defines also TSV side metal pads, metal re-distribution	max. Temp: 420°C. Wafer exposed to vacuum, several process gases, solvent cleans
AMS	8" wafer	2nd temporary handling wafer bonding	bonded on TSV-side		

AMS	8" wafer	removal of 1st temporay handling wafer	exposes WG-side again		
AMS	8" wafer	WG side Padmask	opening of Al-Pads on WG-side	ev. also areas of grating coupler will be cleared of passivation nitride by this maskin step	
AMS	8" wafer	de-bonding of 2nd temporary handling wafer	Option: IZM re-uses temporary bonded wafer stack Otherwise: AMS delivers wafer on foil to IZM	pre evaluations planned if AMS de-bonded: WG slots have to be/stay clean	shipment of thin interposer wafer AMS-IZM
IZM	8" wafer	bonding of temporary handling wafer	temporary handling wafer on TSV side necessary. Refer to option of re-use of AMS handling wafer	pre evaluations planned	
IZM	8" wafer	UBM	UBM , Cu / Ni /Au on WG side	TSV side protected	
IZM	8" wafer	deposition of stud bumps	stud bumps on TSV side		
IZM	8" wafer	de-bonding of temporary handling wafer		high topology on WG side due to 50µm UBM thickness	
IZM	8" wafer	singulation	dicing of interposer wafer	TSV side protected by dicing tape	
IZM	die	stud bumping	on WG side	specific tooling required for double sided stud bumping	
IZM	die	bonding of TIA, Driver	thermo compression bonding of components on TSV-side		
IZM	die	bonding of VCSEL, PD	thermo compression bonding of components on WG-side	Thermal and mechanical stress must not be harmful to VCSEL/PD	VCSEL and PD arrays must withstand forces and temperature at 260°C
IZM	die	Mounting of interposer on PCB	thermo compression bonding of interposer on PCB		Max. Temp: 260°C for TC bonding

2.5.2 Critical Steps

- Sending of wafers back and forth between AMO and AMS several times necessary

2.6 *Risk Assessment*

Table 5 shows the evaluation of the critical steps found in the different process flow versions (SOH, Carrier Depletion 150mm, Carrier Depletion ePIX, Carrier Depletion AMO-AMS). The most risks were found in the process flows involved in the silicon organic hybride technology and the carrier depletion switches on 150mm by UPVLC. The first because the wave guide is definitely a very critical critical structures in respect to surface roughness and contamination because of the loss of light power. It turned out to be extremely disadvantageous to open this structure after a first coverage with a Si oxide cladding layer and to do a series of further processing steps with this exposed wave guide window. The second flow is less critical in respect to the wave guide structure, but the combination of 150mm with 200mm wafers demands the development of numerous

special steps just to enable the combined processing, which is of no practical benefit, but could turn to show stoppers.
The final decision is depicted in table 6. The process with the most robust process flow and the lowest risk is the realization of carrier depletion switches on 200mm wafers by a cooperation of AMO and AMS.

Table 5: Evaluation of the 4 different process flows

process option	Risk Statement	P	I	Risk Severity (P*I+I)	Response Category
SOH	wave guide surface damage during opening of WG window	2	5	15	Mitigate
SOH	bonding voids during first temp. Wafer bonding because of large WG openings	4	5	25	Transfer
SOH	wave guide surface damage during temporary bonding or de-bonding	3	4	16	Mitigate
SOH	wave guide surface damage during tape sticking and removal process	2	4	12	Accept
SOH	contamination of wave guide surface during stud bump process or thermo compression bonding	3	4	16	Mitigate
SOH	deposition of organic layer on single chips bonded to PCB results misprocessed cladding	3	5	20	Transfer
SOH	processing of single chips bonded to PCB is not mass production capable	5	4	24	Transfer
Carrier depletion UPVLC (150mm)	back-end processing at UPVLC is not established and will not work	3	4	16	Mitigate
Carrier depletion UPVLC (150mm)	metallization needed for TSV landing pads not optimized	3	4	16	Mitigate
Carrier depletion UPVLC (150mm)	planarization needed for bonding of first handling wafer will not completely developed	3	4	16	Mitigate
Carrier depletion UPVLC (150mm)	thinning of 150mm on 200mm handling wafer, risk of handling wafer damage	4	5	25	Transfer
Carrier depletion UPVLC (150mm)	Stack of 150mm wafer and 200mm wafer has a high step, risk of etch damages	5	4	24	Transfer
Carrier depletion UPVLC (150mm)	Temp bonding of 150mm/200mm wafer stack to 200mm wafer results in a 25mm wide region with gap, handling wafer removal with wafer breakage likely	4	4	20	Transfer
Carrier depletion UPVLC (150mm)	De-bonding of 150mm wafer from 200mm handling wafer by external supplier	5	3	18	Mitigate
Carrier depletion ePIX (200mm)	Contacts at AMS to be processed to Ni Silicide: cross contamination risk	2	2	6	Contingency

Carrier depletion ePIX (200mm)	Cost issue	5	5	30	avoid
Carrier depletion AMO-AMS (200mm)	Sending of wafers back and forth between AMO and AMS several times necessary	5	1	6	Contingency

Table 6: Final decision for the carrier depletion technology processed by AMO and AMS

Photonic switching technology	Silicon photonics Fab	Wafer size	Risk level	Main topic for integration	Other
SOH type (KIT)	AMO	6" (8")	HIGH	Polymer temperature stability	
Carrier depletion pn type (UPVLC)	UPVLC	6"	HIGH	Wafer size incompatibility	
Carrier depletion pn type (UPVLC)	ePIXFab service (IMEC)	8"	MEDIUM	Fab Cross-Contamination	Costs too high
Carrier depletion pn type (UPVLC)	AMO	6" (8")	LOW	8" structuring @ AMO	